RECEIVED
CENTRAL FAX CENTER
MAY 23 2006

ONS00507
10/797,537

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: :

Rajesh S. Nair et al. :

Serial No.: 10/797,537 : Examining Group: 2822

Filed: March 11, 2004 : Examiner: Kiesha L. Rose

For: **HIGH VOLTAGE LATERAL FET STRUCTURE WITH IMPROVED ON RESISTANCE PERFORMANCE**

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, attn: Examiner **Kiesha L. Rose**

FAX No. (571) 273-8300 on May 23, 2006

By Signature: Lydia McNamara

Lydia McNamara (602.244.5603)

30 pages

APPEAL BRIEF

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Semiconductor Components Industries, LLC (SCI), doing business as ON Semiconductor.

05/24/2006 STEUMEL1 00000040 501086 10797537

01 FC:1402 500.00 DA

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals or interferences to this application.

III. STATUS OF THE CLAIMS

Claims 1-6, and 8-21 are in the proceeding, and are the claims on appeal. Claim 7 was cancelled in a previous amendment. A copy of the claims on appeal is provided in Section VIII., Claims Appendix.

Claim 7 was cancelled.
Claims 1-6, and 8-21 are rejected.

IV. STATUS OF THE AMENDMENTS

An amendment was filed on October 11, 2005 and entered into the record. A Response to a Final Rejection was filed on April 6, 2006 but was not entered into the record.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 calls for a lateral insulated gate field effect transistor (IGFET) device (10, 100, 200), as described on page 3, line 25 through page 10, line 8, and as shown in FIGS. 1-3, comprising a semiconductor substrate (11) having a first conductivity type. By way of example, the substrate (11) is described as p-type on page 3, line 34. As described on page 4, line 5 through line 34, a region of semiconductor material (13) comprising alternating layers (16, 17, 18, 19, and/or 21) of first and second conductivity type material are formed overlying the semiconductor substrate (11) and having a first major surface (14). As described on page 4, lines 25-29, the region of

semiconductor material (13) further includes a top layer (23) of the first conductivity type formed adjacent the first major surface (14) and one of the alternating layers (21) of the second conductivity type formed adjacent and below the top layer (23). As described on page 4, lines 25-29, the top layer (23) sets or determines the blocking voltage of the device. Further, the top layer (23) has the same conductivity type as the substrate (11).

As described on page 5, lines 25-31, a drain region (36) of the second conductivity type extends from the first major surface (14) into at least a portion of the region of semiconductor material (13).

As described on page 6, lines 12-16, a body region (41) of the first conductivity type is formed in a portion of the region of semiconductor material (13) and extends from the first major surface partially into the top layer (23). As claimed, the body region (41) and the top layer (23) have the same conductivity type. A first source region (43) is formed in the body region (41).

As described on page 6, lines 17 through page 7, line 25 a trench gate structure (47, 53, and 54) is formed in a portion of the region of semiconductor material (13) and adjoins the alternating layers (21, 19, 18, 17 and/or 16). As further described on page 6, lines 22-27 and shown in FIG. 1, the trench gate structure (46, 53, and 54) controls a sub-surface channel region (e.g., 57, 571, 572, and/or 573).

As described on page 8, lines 21-31, the IGFET device (10, 100, 200) of claim 1 has a lower R_{ON}*Area than prior art devices because second conductivity type layers 16, 18 and/or 21 provide low resistance paths for current flow. As further described on page 9, lines 10-16, since the body region (41) extends from the first major surface (14) only partially into the top layer (23),

deep diffusion steps are avoided, which saves on space and manufacturing time.

Claim 4 ultimately depends from claim 1 and further calls for a first doped region (223) of the second conductivity type formed adjacent a portion of the sidewall surfaces of the trench gate structure (47) and adjacent to the alternating layers (23, 21, 19, 18, 17 and/or 16). This feature is described on page 9, line 33 through page 10, line 8, and shown in FIG. 3. As described on page 10, lines 6-8, the first doped region (223) reduces resistance in layers 17, 19 and 21, which further reduces the R_{ON}*Area performance of the IGFET device (10, 100 or 200).

Claim 5 calls for the device of claim 1 to further include a surface gate structure (49) including a gate dielectric layer (63) formed overlying the first major surface (14), and a gate electrode layer (64) formed overlying the gate dielectric layer (63). The surface gate structure (49) controls conduction in a surface channel region (58). The surface gate structure (49) is shown in FIGS. 1 and 3. As described on page 8, lines 32-35, the surface gate structure (49) provides for an additional current path (I_1), which provides a further reduction in R_{ON}.

Claim 9 calls for the device of claim 5 to further include a diffused drain extension region (26) of the second conductivity type formed in the top layer 23 and between the body region (41) and the drain region (36). The diffused drain extension region (26) is shown in FIGS. 1 and 3 and further described on page 5, lines 1-7. As described on page 8, lines 32-35, the diffused drain extension region (26) together with the surface gate structure (49) provides for lower R_{ON}.

Claim 10 calls for a lateral MOSFET device (10 and 200), as described on page 3, line 25 through page 10, line 8, and as shown in FIGS. 1 and 3, comprising a semiconductor substrate (11) having a first conductivity type. By way of example, the substrate (11) is described as p-type on page 3, line 34. As described on page 3, line 35 through page 4, line 35 and shown in FIGS. 1 and 3, a region of semiconductor material (13) including a plurality of alternating layers of first and second conductivity semiconductor material (16, 17, 18, 19, 21, and/or 23) is formed over semiconductor substrate (11). The region of semiconductor material (13) includes a major surface (14).

The device (10 and 200) also includes a trench drain structure (36), which is described on page 5, line 25 to page 6, line 11 and shown in FIGS. 1 and 3. The trench drain structure (36) is formed in the region of semiconductor material (13).

As described on page 6, line 17 through page 8, line 13 and shown in FIGS. 1 and 3, the device (10 and 200) of claim 10 further includes a trench gate structure (47) formed in the region of semiconductor material (13) and a surface gate structure (49) including a gate dielectric layer (63) and a gate conductive portion (64) formed overlying the major surface (14).

As described on page 6, lines 12-16, the device (10 and 200) further includes a body region (41) of the first conductivity type formed adjacent the trench gate structure (47) and the surface gate structure (49), and a source region (43) of the second conductivity type formed in the body region (41). As described on page 8, line 21 to page 9, line 4, a feature the device (10 and 200) of claim 10 is that second conductivity type layers of the region of semiconductor material (13) provide low resistance paths for current to flow, which reduces R_{ON} of the device (10 and 200) without increasing area. Additionally, the surface gate structure (49) provides an additional current path (I_1) (described on page 8, lines 32-34), which further reduces R_{ON}.

In **claim 11**, the device (10 and 200) of claim 10 is defined to further include a diffused drain extension region (26) of the second conductivity type, which is described on page 5, lines 1-7 and further shown in FIGS. 1 and 3. The drain extension region (26) is formed in a portion of the region of semiconductor material (13) and extends from the major surface (14). As described on page 5, lines 7-16 and shown in FIGS. 1 and 3, claim 11 further calls for a region (27) of the first conductivity type formed within a portion of the diffused drain extension region (26). As further described on page 5, lines 7-16, the region (27) allows for downward depletion of the depletion region when device (10) is in the blocking state, which allows the device (10 and 200) to sustain a higher blocking voltage.

In **claim 12**, the device (200) of claim 10 is defined to further include a doped region (223) of the second conductivity type formed in the region of semiconductor material (13). The doped region (223) is described on page 9, line 33 to page 10, line 8, and further shown in FIG. 3. The doped region (223) is adjacent a portion of the trench gate structure (47) and is below the body region (41). As described on page 10, lines 1-8, the doped region (223) reduces resistance in the second conductivity layers (17, 19, and/or 21) of the region of semiconductor material (13) when the device (200) is conducting current in the on state, which further reduces R_{ON}.

Claim 17 calls for an insulated gate FET structure (200), as described on page 9, line 33 to page 10, line 8 and further shown in FIG. 3, comprising alternating layers (16, 17, 18, 19, and/or 21) of first and second conductivity type material forming a semiconductor region (13).

As described on page 6, line 17 through page 8, line 13 and shown in 3, the device (200) of claim 17 further includes a

trench gate structure 47 formed in the alternating layers (16, 17, 18, 19, and/or 21), wherein the trench gate structure (47) controls a sub-surface channel region (57).

The device (200) further includes a body region (41) of the first conductivity type formed in the semiconductor region (13), which is described on page 6, lines 12-16 and further shown in FIG. 3. A drain region (36) of the second conductivity type, which is described on page 5, line 25 through page 6, line 11 and shown in FIG. 3, is formed in the semiconductor region (13) and spaced apart from the trench gate structure (47) and extends into the alternating layers (16, 17, 18, 19, and/or 21). A source region (43) of the second conductivity type is formed in the body region (41) and adjacent the trench gate structure (47).

The device (200) still further includes a doped region (223) of the second conductivity type, which is described on page 9, line 33 to page 10, line 8 and shown in FIG. 3. The doped region (223) is formed along a sidewall of the trench gate structure (47) and extends into the semiconductor region (13) below the body region (41) and adjacent the alternating layers (16, 17, 18, 19, and/or 21). As described on page 10, lines 1-8, the doped region (223) reduces resistance in the second conductivity layers (17, 19, and/or 21) of the region of semiconductor material (13) when the device (200) is conducting current in the on state, which further reduces R_{ON}.

In **claim 21**, the device (200) of claim 17 is defined to further include a top layer (23) formed over one of the alternating layers to form an upper major surface (14), which is shown in FIG. 3. As described on page 4, lines 29-34, the top layer (23) is defined to be thicker than the alternating layers (16, 17, 18, 19 and/or 21). As described on page 5, lines 1-7 and shown in FIG. 3, an extended drain region (26) of the second conductivity type is formed in a portion of the top layer (23)

and extends partially into the top layer (23) from the upper major surface (14).

As described on page 6, lines 17-27 and page 7, lines 26-35 and further shown in FIG. 3, the device (200) further includes a surface gate portion (49) including a gate dielectric portion (63) overlying the upper major surface (14) of the semiconductor region (13) and a gate conductive portion (64) overlying the gate dielectric portion (63). As set forth in claim 21 and shown in FIG. 3, the surface gate portion (49) controls a channel (58) for conducting current (I1) in proximity to the upper major surface (14). As described on page 8, lines 32-35, the surface gate structure (49) provides for an additional current path (I_1), which provides a further reduction in R_{ON}.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejection of claim 11 under 35 U.S.C. §112, second paragraph.

B. Rejection of claims 1-6 and 8-21 under 35 U.S.C. §103 as being unpatentable over Tihanyi, USP 6,507,071, (hereinafter "Tihanyi") in view of Disney, USP 6,509,220, (hereinafter "Disney").

VII. ARGUMENT

A. Argument traversing rejection of claim 11 under 35 U.S.C. §112, second paragraph.

Claim 11 was rejected under §112, second paragraph because the Examiner alleges that it is unclear what the region of the first conductivity type is and how it is formed in a portion of

the diffused drain extension region. Applicants respectfully traverse this rejection.

In view of the description in applicants' specification on page 5, lines 1-16, this region is described in one embodiment as p-top region 27, which is further shown in FIG. 1. As shown in FIG. 1, this example of the present invention shows region 27 within a portion of diffused drain extension region 26. By "portion" in this example, p-top region 27 does not occupy all of or extend throughout diffused drain extension region 26.

In view of the above, applicants respectfully submit that claim 11 meets the requirements of §112, second paragraph and that the rejection of claim 11 on such grounds has been traversed.

B. Arguments for allowability of Claims 1-6 and 8-21 over Tihanyi in view of Disney.

1. Arguments for allowability of Claims 1, 2-3, and 8

Claim 1 calls for a lateral IGFET device comprising a semiconductor substrate having a first conductivity type. A region of semiconductor material comprising alternating layers of first and second conductivity type material is formed over the semiconductor substrate and has a first major surface, the region of semiconductor material further includes a top layer of the first conductivity type formed adjacent the first major surface and one of the alternating layers of the second conductivity type formed adjacent and below the top layer. A drain region of the second conductivity type extends from the first major surface into at least a portion of the region of semiconductor material. A body region of the first conductivity type is formed in a portion of the region of semiconductor material and extending

from the first major surface partially into the top layer. A first source region is formed in the body region, and a trench gate structure is formed in a portion of the region of semiconductor material and adjoining the alternating layers, wherein the trench gate structure controls a sub-surface channel region.

As set forth in applicants' specification on page 8, lines 21-31, the second conductivity type layers of the present invention provide additional low resistance paths for current to flow without increasing the area of the device, which reduces R_{ON}*Area. As further set forth on page 9, lines 10-16, the present invention as set forth in claim 1 allows for the body region to extend only partially into the top layer, which allows for smaller cell sizes and reduced manufacturing cycle times.

a. Applicants submit that there is no motivation to combine the Tihanyi and Disney references.

It is widely accepted that in order for a prima facie case to stand under 35 U.S.C. §103(a), there must be motivation to combine the references cited. Where a proposed modification would destroy the function of a reference, this is strong evidence against motivation to combine. In re Haruna 249, F.3d 1327, 58 U.S.P.Q.2d 1517 (Fed. Cir. 2001). Further, if there is conflict between the references, such conflict goes against motivation to combine. In re Young 927 F.2d 588, 591, 18 U.S.P.Q.2d 1089, 1091 (Fed. Cir. 1991).

Applicants respectfully submit that there is no motivation to combine the Tihanyi and Disney because the proposed combination of references would destroy the function of a reference, or in the alternative, there is direct conflict between the teachings of the two references. Specifically, in Tihanyi, the alternating layers 3 and 4 extend between and adjoin

both the gate region 12/14 and the drain region 9. However, in Disney, the alternating p-type buried layers do not adjoin either the gate region nor the drain region. Further, as stated in Disney Column 7, lines 47-60, this is done intentionally in order to improve the breakdown voltage of the Disney embodiment. In fact, Disney expressly states that the "P-type buried layer regions [are] surrounded above, below, and laterally by N-type material." Based on at least this express statement, applicants respectfully submit that there is no motivation to combine the references for any purposes because the function of the Disney device would be destroyed (i.e., degradation in breakdown voltage), or because there is direct conflict (i.e., degradation in breakdown voltage) between the teachings of the two references.

In view of the above, applicants respectfully believe that a prima facie case of obviousness has not been presented, and that claim 1 is allowable for at least this reason.

b. Even if motivation existed, the two references still fail to show or suggest each element set forth in claim 1.

Assuming arguendo that there is motivation to combine the references, applicants respectfully submit that the combination of Tihanyi and Disney still fails to make claim 1 obvious. Claims 1 calls for a body region (41) of a first conductivity type to be formed extending partially into a top layer (23) that is also the first conductivity type. In Tihanyi, the body region (11) extends through all of the layers into the underlying substrate (1). In Disney, body region 40 is P-type, and it is formed in an N-type layer (10 70 or 120). Further Disney does not suggest changing the conductivity type so that the body

region and the top layer are the same type as is called for in claim 1.

Thus, applicants respectfully submit that claim 1 is allowable for this additional reason.

Claims 2, 3 and 8 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

2. Arguments for allowability of Claim 4.

Claim 4 depends from claim 3 and further calls for a first doped region of the second conductivity type formed adjacent a portion of the sidewall surfaces and adjacent the alternating layers. As stated in applicants' specification on page 10, lines 6-8, this doped region reduces resistance in the alternating layers when the device is conducting current, which further reduces R_{ON} and R_{ON}*Area.

Claim 4 is believed allowable for the same reasons as claim 1. The present Office Action erroneously relies on region 41 in Disney's FIG. 6 to teach the elements of claim 4. However, as is clearly evident in FIG. 6, region 41 is not adjacent a portion of the sidewall surfaces of the trench gate because there is no trench gate in FIG. 6. Further, Disney's region 41 clearly does not extend below body region 40 as is expressly called for in claim 4, but instead lies strictly within Disney's body region 40. In addition, Disney's region 41 and body region 40 are the same conductivity type (i.e., first conductivity type), while claim 4 expressly calls for the first doped region to be a second conductivity type. Thus, applicants respectfully submit that claim 4 is allowable for these additional reasons.

3. Arguments for allowability of Claim 5.

Claim 5 depends from claim 1 and further calls a surface gate structure including a gate dielectric layer formed overlying the first major surface and a gate electrode layer overlying the gate dielectric layer, wherein the surface gate structure controls conduction in a surface channel region. Claim 5 is believed allowable for the same reasons as claim 1.

Additionally, applicants respectfully submit that the Examiner has resorted to using their specification as a roadmap to pick and choose elements from the Disney reference when there is no motivation to do so absent their invention. Applicants further submit that such a practice is not appropriate to establish a rejection under §103(a). Yamanouchi Pharmaceutical Co., Ltd. V. Danbury Pharmacal, Inc., 231 F.3d 1339, 56 U.S.P.Q.2d 1641 (Fed. Cir.), reh'g denied, 2000 U.S. App. LEXIS 34047 (2000) ("Applicant's specification cannot be basis for motivation to combine"). Further, it is accepted that an ability to modify is insufficient. In re Laskowski, 871 F.2d 115, 117, 10 U.S.P.Q. 1397, 1399 (Fed. Cir. 1989).

Claim 5 expressly calls for a structure having both a trench gate structure adjoining the first source region for controlling a sub-surface channel and a surface gate structure adjoining the first source region for controlling a surface channel.

It is clear that Tihanyi shows only a trench gate structure for controlling a sub-surface channel, and makes absolutely no suggestion to further include a surface gate structure for controlling a surface channel as called for in claim 1.

Additionally, Disney's FIG. 5 embodiment shows only a trench gate 63/64 for controlling a sub-surface channel, and Disney's FIG. 6 embodiment shows only a planar gate 44 for controlling a surface channel. When describing these two figures, Disney

expressly states at column 8 lines 38-62 that FIGS. 5 and 6 are alternative embodiments that "involve replacing the gate and/or drain regions of the device with trench structures." No where does Disney show or suggest using both a planar gate and a trench gate in the same device as is called for in claim 5. Applicants respectfully submit that the term "replace" means to substitute, not to add, and this term actually teaches away from their invention.

Moreover, applicants submit that Disney's FIG. 12 embodiment cannot be used either because the surface structure in FIG. 12 is not a gate used to control a surface channel as called for in claim 1 because Disney's surface structure does not extend over source region 52. It only extends over body contact 151, which is the same conductivity type as p-body 130. Thus, there is no surface channel in FIG. 12 at all - only a vertical sub-surface channel controlled by trench gate 153/154. For these additional reasons, applicants submit that claim 5 is allowable over the cited references.

4. Arguments for allowability of Claim 9.

Claim 9 depends from claim 5 and further calls for a diffused drain extension region of the second conductivity type formed in the top layer and between the body region and the drain region. Claim 9 is believed allowable for the same reasons as claims 1 and 5. Additionally, applicants respectfully submit that claim 9 is allowable because neither Tihanyi nor Disney show or suggest a drain extension region of the second conductivity type formed in the top layer between the body the region and drain region. In fact, both references are completely silent on drain extension regions. Thus, applicants respectfully submit that claim 9 is allowable for this additional reason.

5. Arguments for the allowability of claims 10, and 13-16.

Claim 10 calls for a lateral MOSFET device comprising a semiconductor substrate and a region of semiconductor material including a plurality of alternating layers of first and second conductivity semiconductor material formed over the semiconductor substrate and having a major surface. A trench drain structure is formed in the region of semiconductor material. A trench gate structure is formed in the region of semiconductor material, and a surface gate structure including a gate dielectric layer and a gate conductive portion is formed overlying the major surface. A body region of first conductivity type is formed adjacent the trench gate structure and the surface gate structure, and a source region of the second conductivity type is formed in the body region.

a. Applicants first submit that there is no motivation to combine the Tihanyi and Disney.

Applicants first submit that there is no motivation to combine Tihanyi and Disney because the proposed combination of references would destroy the function of a reference, or in the alternative, there is direct conflict between the teachings of the two references. Specifically, in Tihanyi, the alternating layers 3 and 4 extend between and adjoin both the gate region 12/14 and the drain region 9. However, in Disney, the alternating p-type buried layers do not adjoin either the gate region nor the drain region. Further, as stated in Disney column 7, lines 47-60, this is done intentionally in order to improve the breakdown voltage of the Disney embodiment. In fact, Disney expressly states that the "P-type buried layer regions [are] surrounded above, below, and laterally by N-type material."

Based on this express statement, applicants respectfully submit that there is no motivation to combine the references for any purposes because the function of the Disney device would be destroyed (i.e., degradation in breakdown voltage), or because there is direct conflict (i.e., degradation in breakdown voltage) between the teachings of the two references.

In view of the above, applicants respectfully submit that a prima facie case of obviousness has not been presented, and that claims 10-16 are allowable for at least these reasons.

b. Even if motivation existed, the two references still fail to show or suggest each element set forth in claim 10.

Assuming arguendo that there is motivation to combine the references, applicants respectfully submit that the Examiner has resorted to using their specification as a roadmap to pick and choose elements from the Disney reference when there is no motivation to do so absent their invention. Applicants further submit that such a practice is not appropriate to establish a rejection under §103(a). Yamanouchi Pharmaceutical Co., Ltd. V. Danbury Pharmacal, Inc., 231 F.3d 1339, 56 U.S.P.Q.2d 1641 (Fed. Cir.), reh'g denied, 2000 U.S. App. LEXIS 34047 (2000) ("Applicant's specification cannot be basis for motivation to combine"). Further, it is accepted that an ability to modify is insufficient. In re Laskowski, 871 F.2d 115, 117, 10 U.S.P.Q. 1397, 1399 (Fed. Cir. 1989).

Among other things, claim 10 expressly calls for a trench drain and both a trench gate structure and a surface gate structure. It is clear that Tihanyi only shows a trench gate structure, and makes absolutely no suggestion to further include a surface gate structure for controlling a surface channel. Additionally, Disney's FIG. 5 embodiment shows only a planar

drain 47 with a trench gate 63/64, and Disney's FIG. 6 embodiment shows only a trench drain 67 with a planar gate 44. When describing these two figures, Disney expressly states at column 8 lines 38-62 that FIGS. 5 and 6 are alternative embodiments that "involve replacing the gate and/or drain regions of the device with trench structures." No where does Disney show or suggest using both a planar gate and a trench gate in the same device as is called for in claim 10. Applicants respectfully submit that the term "replace" means to substitute, not to add, and this term actually teaches away from their invention.

Moreover, applicants submit that Disney's FIG. 12 embodiment cannot be used either because the surface structure in FIG. 12 is not a gate used to control a surface channel as called for in claim 10 because Disney's surface structure is not adjacent source region 52. It is adjacent body contact 151 only, which is the same conductivity type as p-body 130. Thus, there is no surface channel in FIG. 12 at all, only a vertical sub-surface channel controlled by trench gate 153/154. For at least these reasons, applicants submit that claim 10 is allowable over the cited references.

Claims 13-16 depend from claim 10 and are believed allowable for at least the same reasons as claim 10.

6. Arguments for the allowability of claim 11.

Claim 11 depends from claim 10 and further calls for a diffused drain extension region of the second conductivity type formed in a portion of the region of semiconductor material and extending from the major surface, and a region of the first conductivity type formed within a portion of the diffused drain extension region. Applicants respectfully submit that claim 11 is allowable for at least the same reasons as claim 10.

Additionally, applicants respectfully submit that claim 11 is allowable because neither Tihanyi nor Disney show or suggest a diffused drain extension region nor a region of the first conductivity type formed within a portion of the diffused drain extension region. In fact, both references are completely silent on these elements. Thus, applicants respectfully submit that claim 11 is allowable for this additional reason.

7. Arguments for the allowability of claim 12.

Claim 12 depends from claim 10 and further calls for a doped region of the second conductivity type formed in the region of semiconductor material adjacent a portion of the trench gate structure and below the body region. As stated in applicants' specification on page 10, lines 6-8, this doped region reduces resistance in the alternating layers when the device is conducting current, which further reduces R_{ON} and R_{ON}*Area.

Applicants respectfully believe that claim 12 is allowable for at least the same reasons as claim 10. Additionally, applicants respectfully submit that claim 12 is allowable over Tihanyi and Disney because neither reference shows or suggests the doped region called for in claim 12. The present Office Action appears to rely on region 41 in Disney's FIG. 6 to teach this element. However, as is clearly evident in FIG. 6, Disney's region 41 is not below body region 40 as is expressly called for in claim 12, but instead lies strictly within the body region. In addition, Disney's region 41 and body region 40 are the same conductivity type (i.e., first conductivity type), while claim 12 expressly calls for the doped region to be a second conductivity type. Thus, applicants respectfully submit that claim 12 is allowable for these additional reasons.

8. Arguments for the allowability of claims 17 and 18-20.

Claim 17 calls for an insulated gate FET structure comprising alternating layers of first and second conductivity type material forming a semiconductor region. A trench gate structure is formed in the alternating layers, wherein the trench gate structure controls a sub-surface channel region. A body region of the first conductivity type is formed in the semiconductor region adjacent the trench gate structure. A drain region of the second conductivity is formed in the semiconductor region and spaced apart from the trench gate structure and extends into the alternating layers. A source region of the second conductivity type is formed in the body region and adjacent to the trench gate structure. A doped region of the second conductivity type formed along a sidewall of the trench gate structure and extending into the semiconductor region below the body region.

a. Neither Tihanyi nor Disney show or suggest at least two express elements set forth in claim 17.

Applicants respectfully submit that neither Tihanyi nor Disney show or suggest at least a doped region of the second conductivity type formed along a sidewall of the trench gate structure and extending into the semiconductor region below the body region. The present Office Action appears to rely on region 41 in Disney's FIG. 6 to teach this element. However, as is clearly evident in FIG. 6, Disney's region 41 is not below body region 40 as is expressly called for in claim 12, but instead lies strictly within the body region. Further, Disney's region 41 is the same conductivity type as body region 40 (i.e., the first conductivity type), which is not a second conductivity type as is called for in claim 17. Thus, for at least these reasons,

applicants respectfully submit that claim 17 is allowable over Tihanyi in view of Disney.

Claims 18-20 depend from claim 17 and are believed allowable for at least the same reasons as claim 17.

9. Arguments for the allowability of claim 21.

Claim 21 depends from claim 17 and further calls for, among other things, a top layer formed over one of the alternating layers to form an upper major surface of the semiconductor region, wherein the top layer is thicker than the alternating layers of first and second conductivity type. An extended drain region of the second conductivity type is formed in a portion of the top layer and extending partially into the top layer from the upper major surface. A surface gate portion including a gate dielectric layer is formed overlying the upper major surface of the semiconductor region and a gate conductive portion overlying the gate dielectric portion, wherein the surface gate portion controls a channel for conducting current at the upper major surface.

Claim 21 is believed allowable for the same reasons as claim 17. Also, applicants respectfully submit that claim 21 is allowable because neither Tihanyi nor Disney show or suggest a extended drain region formed in the top layer. In fact, both references are completely silent on this element.

Additionally, applicants respectfully submit that the Examiner has resorted to using their specification as a roadmap to pick and choose elements from the Disney reference when there is no motivation to do so absent their invention. Applicants further submit that such a practice is not appropriate to establish a rejection under §103(a). Yamanouchi Pharmaceutical Co., Ltd. V. Danbury Pharmacal, Inc., 231 F.3d 1339, 56

U.S.P.Q.2d 1641 (Fed. Cir.), reh'g denied, 2000 U.S. App. LEXIS 34047 (2000) ("Applicant's specification cannot be basis for motivation to combine"). Further, it is accepted that an ability to modify is insufficient. In re Laskowski, 871 F.2d 115, 117, 10 U.S.P.Q. 1397, 1399 (Fed. Cir. 1989).

Claim 21 expressly calls for a structure having both a trench gate structure for controlling a sub-surface channel and a surface gate structure for controlling a channel for conducting current in proximity to the upper major surface.

It is clear that Tihanyi shows only a trench gate structure for controlling a sub-surface channel, and makes absolutely no suggestion to further include a surface gate structure for controlling a surface channel as called for in claim 1.

Additionally, Disney's FIG. 5 embodiment shows only a trench gate 63/64 for controlling a sub-surface channel, and Disney's FIG. 6 embodiment shows only a planar gate 44 for controlling a surface channel. When describing these two figures, Disney expressly states at column 8 lines 38-62 that FIGS. 5 and 6 are alternative embodiments that "involve replacing the gate and/or drain regions of the device with trench structures." No where does Disney show or suggest using both a planar gate and a trench gate in the same device as is called for in claim 5. Applicants respectfully submit that the term "replace" means to substitute, not to add, and this term actually teaches away from their invention.

Moreover, applicants submit that Disney's FIG. 12 embodiment cannot be used either because the surface structure in FIG. 12 is not a gate used to control a surface channel as called for in claim 1 because Disney's surface structure does not extend over source region 52. It only extends over body contact 151, which is the same conductivity type as p-body 130. Thus, there is no surface channel in FIG. 12 at all - only a vertical sub-surface

channel controlled by trench gate 153/154. For these additional reasons, applicants submit that claim 21 is allowable over the cited references.

In view of the above, it is believed that the claims are allowable, and the Board of Appeals and Interferences is respectfully requested to reverse the Examiner.

Respectfully submitted,

Rajesh S. Nair et al.

ON Semiconductor
Intellectual Property Dept.
P.O. Box 62890; M/D A700
Phoenix, AZ 85082-2890

Kevin B. Jackson
Attorney for Applicants
Reg. No. 38,502
Tel. (602) 244-4885

Date: May 23, 2006

VIII. CLAIMS APPENDIX

1. (previously presented): A lateral IGFET device comprising:

a semiconductor substrate having a first conductivity type;

a region of semiconductor material comprising alternating layers of first and second conductivity type material formed overlying the semiconductor substrate and having a first major surface, the region of semiconductor material further including a top layer of the first conductivity type formed adjacent the first major surface and one of the alternating layers of the second conductivity type formed adjacent and below the top layer;

a drain region of the second conductivity type extending from the first major surface into at least a portion of the region of semiconductor material;

a body region of the first conductivity type formed in a portion of the region of semiconductor material and extending from the first major surface partially into the top layer;

a first source region formed in the body region; and

a trench gate structure formed in a portion of the region of semiconductor material and adjoining the alternating layers, wherein the trench gate structure controls a sub-surface channel region.

2. (original): The device of claim 1 wherein in the drain region comprises a trench filled with a doped polycrystalline material.

3. (original): The device of claim 1 wherein the trench gate structure is filled with a doped polycrystalline material of the second conductivity type, and wherein the trench gate structure extends from the first major surface adjacent the source region and a portion of the body region into the region of semiconductor material, and wherein the trench gate includes a first gate dielectric layer formed at least on sidewall surfaces of the trench gate structure.

4. (previously presented): The device of claim 3 further comprising a first doped region of the second conductivity type formed adjacent a portion of the sidewall surfaces and adjacent the alternating layers.

5. (previously presented): The device of claim 1 further comprising a surface gate structure including a gate dielectric layer formed overlying the first major surface and a gate electrode layer overlying the gate dielectric layer, wherein the surface gate structure controls conduction in a surface channel region.

6. (original): The device of claim 1 wherein a lower portion of the trench gate structure terminates within the semiconductor substrate.

7 (cancelled): The device of claim 1 wherein one layer of the alternating layers adjacent the first major surface comprises the first conductivity type.

8. (previously presented): The device of claim 1 wherein the top layer is thicker than adjacent layers in the region of semiconductor material.

9. (currently amended): The device of claim 5 further comprising a diffused drain extension region of the second conductivity type formed in the top layer and between the body region and the drain region.

10. (previously presented): A lateral MOSFET device comprising:

a semiconductor substrate;

a region of semiconductor material including a plurality of alternating layers of first and second conductivity semiconductor material formed over the semiconductor substrate and having a major surface;

a trench drain structure formed in the region of semiconductor material;

a trench gate structure formed in the region of semiconductor material;

a surface gate structure including a gate dielectric layer and a gate conductive portion formed overlying the major surface;

a body region of first conductivity type formed adjacent the trench gate structure and the surface gate structure; and

a source region of the second conductivity type formed in the body region.

11. (previously presented): The lateral MOSFET device of claim 10 further comprising a diffused drain extension region of the second conductivity type formed in a portion of the region of semiconductor material and extending from the major surface, and a region of the first conductivity type formed within a portion of the diffused drain extension region.

12. (previously presented): The lateral MOSFET device of claim 10 further comprising a doped region of the second conductivity type formed in the region of semiconductor material adjacent a portion of the trench gate structure and below the body region.

13. (original): The lateral MOSFET device of claim 10 wherein the region of semiconductor material includes a layer of the first conductivity type at the major surface, and wherein the layer has a thickness greater than adjacent layers within the region of semiconductor material.

14. (original): The lateral MOSFET device of claim 10 wherein at least a portion of the alternating layers within the region of semiconductor material extend between the trench drain structure and the trench gate structure.

15. (original): The lateral MOSFET device of claim 10 wherein the trench drain structure includes a trench filled with a polycrystalline semiconductor material having the second conductivity type.

16. (original): The lateral MOSFET device of claim 10 wherein the trench gate structure extends further into the region of semiconductor material than the trench drain structure.

17. (previously presented): An insulated gate FET structure comprising:

alternating layers of first and second conductivity type material forming a semiconductor region;

a trench gate structure formed in the alternating layers, wherein the trench gate structure controls a sub-surface channel region;

a body region of the first conductivity type formed in the semiconductor region adjacent the trench gate structure;

a drain region of the second conductivity formed in the semiconductor region and spaced apart from the trench gate structure and extending into the alternating layers;

a source region of the second conductivity type formed in the body region and adjacent to the trench gate structure; and

a doped region of the second conductivity type formed along a sidewall of the trench gate structure and extending into the semiconductor region below the body region and adjacent the alternating layers.

18. (original): The insulated gate FET structure of claim 17 wherein the drain region comprises a trench filled with a polycrystalline semiconductor material.

19. (original): The insulated gate FET structure of claim 18 wherein the trench gate structure extends into the alternating layers deeper than the drain region.

20. (original): The insulated gate FET structure of claim 17 wherein the trench gate structure controls a plurality of sub-surface channel regions.

21. (previously presented): The insulated gate FET structure of claim 17 further comprising:

a top layer of the second conductivity formed over one of the alternating layers of the first conductivity type to form an upper major surface of the semiconductor region, wherein the top layer is thicker than the alternating layers of first and second conductivity type;

an extended drain region of the second conductivity type formed in a portion of the top layer and extending partially into the top layer from the upper major surface; and

a surface gate portion including a gate dielectric layer overlying the upper major surface of the semiconductor region and a gate conductive portion overlying the gate dielectric portion, wherein the surface gate portion controls a channel for conducting current in proximity to the upper major surface.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to § 1.130, 1.131, 1.132.

X. RELATED PROCEEDINGS APPENDIX

The appellant is not aware of any related proceedings.

RECEIVED
CENTRAL FAX CENTER
MAY 23 2006

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Appliation Number	10/797537
Filing Date	March 11, 2004
First Named Inventor	Rajesh S. Nair et al.
Examiner Name	Kiesha L. Rose
Art Unit	2822
Attorney Docket No.	ONS00507

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 501086

Deposit Account Name: Semiconductor Components Industries, L.L.C.

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	500.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) 1811 1 20(1) Certificae of Correction

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 500.00

SUBMITTED BY				(Complete *if applicable*)	
Name (Print/Type)	Kevin B. Jackson	Registration No. (Attorney/Agent)	38,502	Telephone	(602) 244-4885
Signature				Date	5/23/2006

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.